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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	Manoj Khare et al.
SERIAL NO.	:	09/749,660
FILED	:	December 28, 2000
FOR	:	METHOD AND APPARATUS FOR REDUCING MEMORY LATENCY IN A CACHE COHERENT MULTI-NODE ARCHITECTURE
GROUP ART UNIT	:	2186
EXAMINER	:	Tuan V. Thai
ASSIGNEE	:	INTEL CORPORATION

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.312

Sir:

Applicants request that the application be amended as shown below to correct a error in claim 29.

Amendments to the Claims begin on page 2.

Remarks begin on page 9.